CLAIMS:

What is claimed is:

1. (Cancelled) A method of forming a multilayer circuit board having inverted microvias, comprising the steps of:

providing at least a first substrate core and a second substrate core each of said first substrate core and said second substrate core having a top conductive layer on at least a top side;

forming a microvia on a bottom side of at least one among the first substrate core and the second substrate core, wherein the microvia would reach to the top conductive layer on at least the top side of at least one among the first substrate core and the second substrate core;

applying a conductive layer to the microvia to interconnect a bottom conductive layer of at least one among the first substrate core and the second substrate core to the top conductive layer of at least one among the first substrate core and the second substrate core;

patterning at least one among the top conductive layer and the bottom conductive layer of at least one among the first substrate core and the second substrate core;

applying an adhesive / bonding layer between at least the first substrate core and the second substrate core;

forming a hole through the first substrate core, the adhesive / bonding layer and the second substrate core; and

applying a conductive layer to the hole to interconnect at least two among the top conductive layer of the first substrate core, the top conductive layer of the second substrate core, the bottom conductive layer of the first substrate core, and the bottom conductive layer of the second substrate core.

2. (Cancelled) The method of claim 1, wherein the step of forming the microvia comprises forming the microvia on the bottom side of the first substrate core and forming a separate microvia on the bottom side of the second substrate core such that each microvia reaches the respective top conductive layer on the first substrate core and the second substrate core.

3. (Cancelled) The method of claim 1, wherein the step of patterning comprises patterning the top conductive layer and the bottom conductive layer of the first substrate core and patterning the top conductive layer and the bottom conductive layer of the second substrate core.

4. (Cancelled) The method of claim 1, wherein the step of applying the adhesive / bonding layer comprises applying a dielectric layer between the bottom layers of the first substrate core and the second substrate core.

5. (Cancelled) The method of claim 1, wherein the step of applying the adhesive / bonding layer comprises applying a dielectric layer on at least exposed portions of the first substrate core and the second substrate core and on at least portions of the bottom conductive layer of the first substrate core and the bottom conductive layer of the second substrate core.

6. (Cancelled) The method of claim 1, wherein the step of forming the microvia comprises the step of at least one among plasma etching, chemical etching, YAG laser drilling, CO_2 laser drilling, and photo imaging.

7. (Cancelled) The method of claim 1, wherein the step of patterning comprises at least one among the steps of plating, applying photolithography, and etching

8. (Cancelled) The method of claim 1, wherein the method further comprises the step of laminating the first substrate core with the second substrate core by curing the adhesive / bonding layer in a vacuum lamination press.

9. (Cancelled) The method of claim 1, wherein the method further comprises the steps of applying an external dielectric layer to at least one among the top conductive layer of the first substrate core and the top conductive layer of the second substrate core.

10. (Cancelled) The method of claim 9, wherein the method further comprises the step of applying an external conductive layer to the external dielectric layer.

11. (Cancelled) The method of claim 10, wherein the method further comprises the step of creating a microvia through at least one among the external dielectric layer and the external conductive layer to expose at least one among the top conductive layer of the first substrate core and the top conductive layer of the second substrate core.

12. (Cancelled) The method of claim 11, wherein the method further comprises applying a conductive layer to the microvia to interconnect the external conductive layer to at least one among the top conductive layer of the first substrate core and the second substrate core.

13. (Cancelled) The method of claim 12, wherein the method further comprises forming a hole through the external conductive layer, the external dielectric layer, as well as the first substrate core, the adhesive / bonding layer and the second substrate core and applying a conductive layer to the hole to interconnect at least two among the external conductive layer, the top conductive layer of the first substrate core, the top conductive layer of the second substrate core, the bottom conductive layer of the first substrate core, and the bottom conductive layer of the second substrate core.

14. (Cancelled) The method of claim 13, wherein the step of patterning comprises at least one among the steps of plating, applying photolithography, and etching.

15. (Original) A multilayer circuit board having inverted microvias, comprising the steps of

at least a first substrate core and a second substrate core each of said first substrate core and said second substrate core having a top conductive layer on at least a top side;

a microvia on a bottom side of at least one among the first substrate core and the second substrate core, wherein the microvia would reach to the top conductive layer on at least the top side of at least one among the first substrate core and the second substrate core;

a conductive layer applied to the microvia interconnecting a bottom conductive layer to the top conductive layer of at least one among the first substrate core and the second substrate core;

an adhesive / bonding layer between at least the first substrate core and the second substrate core;

a hole through the first substrate core, the adhesive / bonding layer and the second substrate core;

a conductive layer applied to the hole to interconnect at least two among the top conductive layer of the first substrate core, the top conductive layer of the second substrate core, the bottom conductive layer of the first substrate core, and the bottom conductive layer of the second substrate core.

16. (Original) The multilayer circuit board of claim 15, wherein at least one among the top conductive layer of the first substrate core, the top conductive layer of the second substrate core, the bottom conductive layer of the first substrate core, and the bottom conductive layer of the second substrate core comprises a predefined pattern.

17. (Original) The multilayer circuit board of claim 15, wherein the multilayer circuit board further comprises an external dielectric layer on at least one among the top side of the first substrate core and the top side of the second substrate core and an external conductive layer on the external dielectric layer.

18. (Original) The multilayer circuit board of claim 17, wherein the hole further goes through the external dielectric layer and the external conductive layer.

19. (Original) The multilayer circuit board of claim 18, wherein the conductive layer applied to the hole interconnects at least two among the top conductive layer of the first substrate core, the top conductive layer of the second substrate core, the bottom conductive layer of the first substrate core, the bottom conductive layer of the second substrate core, and the external conductive layer.

20. (Original) A multilayer circuit board, comprising:

a plurality of substrate cores;

an adhesive / bonding layer between at least two among the plurality of substrate cores;

a microvia in each of at least two of the plurality of substrate cores, wherein the microvia includes a conductive interconnection between a top conductive surface and a bottom conductive surface of each of the at least two of the plurality of substrate cores, wherein at least a microvia in a first substrate core is arranged to be inverted relative to a microvia in a second substrate core; and

a plated through-hole through the plurality of substrate cores and the adhesive / bonding layer, wherein the plated through-hole connects at least two among the top conductive surfaces and the bottom conductive surfaces of the plurality of substrate cores.

21. (Cancelled) The multilayer circuit board of claim 20, wherein the multilayer circuit board further comprises a plated through-hole through the plurality of substrate cores and the adhesive / bonding layer, wherein the plated through-hole connects at least two among the top conductive surfaces and the bottom conductive surfaces of the plurality of substrate cores.

22. (Original) The multilayer circuit board of claim 20, wherein the multilayer circuit board further comprises an external dielectric layer on at least one among a top side of a first substrate core and a top side of a last substrate core and an external conductive layer on the external dielectric layer.

23. (Original) The multilayer circuit board of claim 22, wherein the multilayer circuit board further comprises a plated through-hole through the plurality of substrate cores, the external dielectric layer, and the adhesive / bonding layer, wherein the plated through-hole connects at least two among the external conductive layer, the top conductive surfaces of the plurality of substrate cores, and the bottom conductive surfaces of the plurality of substrate cores.

24. (Added) A multilayer circuit board, comprising:

a plurality of substrate cores;

an adhesive / bonding layer between at least two among the plurality of substrate cores;

a microvia in at least one among the plurality of substrate cores, wherein the microvia includes a conductive interconnection between a top conductive surface and a bottom conductive surface of at least one among the plurality of substrate cores; and

a plated through-hole through the plurality of substrate cores and the adhesive / bonding layer, wherein the plated through-hole connects at least two among the top conductive surfaces and the bottom conductive surfaces of the plurality of substrate cores.